WHERE PASSION
LEADS TO EXCELLENCE

ELSYS
EASTERN EUROPE

MEMBER OF ADVANS GROUP

Based in Belgrade, ELSYS Eastern Europe is a subsidiary of ADVANS Group which is a European group of experts in electronic systems and software. Our 1000 engineers serve a range of industries: in multimedia/wireless, service, medical, network/telecom, energy, aerospace, defense, automotive and IT.

For our offices in **Belgrade**, Serbia, we are looking for:

Analog Mixed-Signal Design and Verification Engineer
2 positions - Internship and permanent job positions

Following good practice from the past years, ELSYS Eastern Europe is announcing open positions for the summer 2018 internships and entry level permanent positions.

Description:

You will be a part of an analog design and modeling team, constituted of engineers with a different level of experience, from experts to juniors. Involvement in analog IP models development, model calibration (model vs schematic) and close interaction with other IC implementation teams in order to achieve IC implementation milestones. Your work on these activities will be challenging and you will have the opportunity to work with industry experts on the state-of-the-art processes, tools, and flows. Selected candidates will receive full training and support from our experienced engineers. The project can be a subject of a bachelor/master thesis or seminar paper.

- Selected candidates will be engaged in:
  - Development of Verilog A/AMS models of AMS IP
  - Analog and mixed-signal circuits analysis
  - Development of AMS design verification environment
  - Using Cadence toolchain for AMS verification
- Intern will receive full training and support from our experienced engineers.
- Internship duration is 4 months, starting in mid-July 2018 or differently defined with candidate
- Full time internship 40h a week or differently defined with candidate
- Internship project can be subject of a bachelor/master thesis or seminar paper
- Interns will receive monthly compensation
- Company will provide accommodation if interns are outside of Belgrade

Qualification Requirements:

- Final year student or fresh graduate with B.Sc. or M.Sc. degree in electrical engineering
- Motivated, proactive, hard working
- Relevant courses/knowledge: basics of analog electronics, VLSI basics
- Skills: Familiar with basic analog circuitry, CMOS, and bipolar technology, VHDL or Verilog HDL language, Cadence tools knowledge is a plus
- Good knowledge of English language

Employee Benefits:

- Integration Program in a Professional, Young & Dynamic Team
- Professional Development Opportunities
- Competitive Salaries & Benefits
- Compensation package includes also Additional Health Insurance, Sport & Social activities
- International Work Environment & Traveling Opportunities

All interested candidates are invited to send **CV and motivation letter in English**, indicating the field of interest, relevant college courses and projects, on the following email: **jobs@elsys-eastern.com**. Deadline for application is **20th May**. Interviews are planned for the **May and June;** the final list of selected candidates will be announced by **18th June**.